UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,120	09/24/2003	Mike Cogdill	200207752-1	7246

22879 7590 03/22/2005

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
JONES, STEPHEN E	

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/671,120	COGDILL ET AL.	
	Examiner	Art Unit	
	Stephen E. Jones	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-5, 7, 8, 10-12, 15-17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buuck et al. in combination with Chi. (both of record)

Buuck (Fig. 2) teaches a transmission line system including: a plurality of receiving devices; a clock signal driver (10) controlling a plurality of devices connected to the line at equal lengths from a distribution point (Claims 10, 11, 17, 19); reflections are attenuated (i.e. overshoot is managed in the same manner as the present invention since reflections are canceled) (Claim 16); and the signals are received concurrently (e.g. see Col. 2, lines 22-26) (Claim 19). Also, note that the circuit is capable of being in

an integrated circuit in the same manner as the present invention, especially since it is the same as the presently claimed structure.

However, Buuck does not teach a termination (Claims 8, 15) stub that is resistive (Claim 1), including a voltage divider having the particulars of Claims 2, 3, 4, 5, 7, 16.

Chi (Fig. 5) teaches a transmission line including: a termination stub having a series resistance and a resistance to ground (i.e. termination voltage, and voltage divider) a driver (Vo); a stub matching system (i.e. a reflection dampening system) formed from a series resistance and a parallel resistance (Zs and Y0) coupled to ground (i.e. steady state voltage) through the parallel resistance (Claims 4-5, 7, 18); a division point (Yd) to a plurality of output path devices (i.e. receivers) (Y1..Yn) (Claim 9).

It would have been considered obvious to one of ordinary skill in the art to have included a termination resistance/divider circuit such as taught by Chi at the distribution point in the Buuck circuit, because it would have provided the advantageous benefit of more precisely reducing reflections at the load of the transmission system, thereby suggesting the obviousness of such a modification. As an obvious consequence of the modification, the combination of Buuck and Chi is the same as the presently claimed structure thus as an obvious consequence would function in the same manner.

4. Claims 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buuck et al. and Chi as applied to claims 1 and 8 above, and further in view of Sato (all of record).

The combination of Buuck and Chi teaches a transmission line and termination as described above. However, they do not explicitly teach the particular resistance means or that the resistance means is a trace resistance and the paths are traces in a circuit board.

Sato provides the general teaching of forming a termination resistance and transmission path as (microstrip) traces, and as would have been well-known in the art providing an additional dielectric layer on top of the traces forms a well-known stripline structure.

It would have been considered obvious to one of ordinary skill in the art to have made the combination of Buuck and Chi circuit as a trace circuit (such as taught by Sato) formed as microstrip or stripline, because it would have been considered a well-known art-recognized equivalent/alternative transmission line system means for forming a terminated circuit.

5. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buuck et al. and Chi as applied to claims 8 and 10-12 above, and further in view of Feraud et al. (all of record).

Buuck and Chi teach a terminated transmission line having driver clock signals (i.e. control signals) as described above, but do not explicitly teach the specific load devices are memory components/chips.

Feraud teaches a similar transmission line system that is controlled by clock signals in which the load devices (i.e. receivers) can be memory chips (e.g. see Col. 1, lines 10-16 and lines 51-55).

Accordingly, it would have been considered obvious to one of ordinary skill in the art to have the generic load devices in the combination of Buuck and Chi to have been memory cards such as taught by Feraud, because it would have been a mere selection of well-known specific load devices based on the desired use of the transmission line system.

Response to Arguments

6. Applicant's arguments filed 12/20/04 have been fully considered but they are not persuasive.

Applicant argues that Chi does not teach communication paths that are the same length and that Chi teaches away from having equal lengths.

Applicant's argument is not convincing, especially since Applicant appears to be arguing the Chi reference alone rather than the combination of Buuck and Chi as applied in the rejections. In the applied rejections it is Buuck that teaches equal lengths. Chi is merely providing a general teaching of a termination means which provides reflection reduction for transmission lines as is well-known in the art of impedance matching.

Applicant also argues that Sato does not teach trace lines on a printed circuit board.

This argument is not persuasive, especially since Sato clearly teaches microstrips and film resistors on a dielectric board (i.e. a printed circuit board).

Additionally, Applicant argues the combination of Buuck and Chi, but does not address the specific motivation as applied in the rejections.

Furthermore, Applicant argues that Feraud does not teach receivers in an IC with control signals that control memory components.

This argument is not convincing since the present claim language does not require an IC but merely requires the device to be capable of functioning in an IC (i.e. integrated circuit is only recited in the preamble). Furthermore, Feraud clearly teaches clock signal controls (i.e. chip select signals).

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen E. Jones whose telephone number is 571-272-1762. The examiner can normally be reached on Monday through Friday from 8 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SEJ

STEPHEN E. JONES
PRIMARY EXAMINER